

AND (0101) Instruction Cycle

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0101				DR			SR1			0	00		SR2		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0101				DR			SR1			1	imm5				

Instruction Fetch

MAR $\leftarrow$ **PC**

PC $\leftarrow$ **PC** + 1

MDR $\leftarrow$ **memory**[**MAR**]

IR $\leftarrow$ **MDR**

Decode

IR[15:12] decoded

Evaluate Address

n/a

Operand Fetch

ALU_{INA} $\leftarrow$ **R**_{IR[8:6]}

ALU_{INB} $\leftarrow$ (**IR**[5] ? **sign_ext**₁₆(**IR**[4:0]) : **R**_{IR[2:0]})

Execute

ALU_{OUT} $\leftarrow$ **ALU**_{INA} and **ALU**_{INB}

Store Result

R_{IR[11:9]} $\leftarrow$ **ALU**_{OUT}